Filed: February 15, 2002

Inventors: Liu, et al.

Docket No.: ACT-322CIP

Page 1 of 23

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FPGA Tile 20

FIG. 1

Filed: February 15, 2002

Inventors: Liu, et al.
Docket No.: ACT-322CIP

Page 2 of 23

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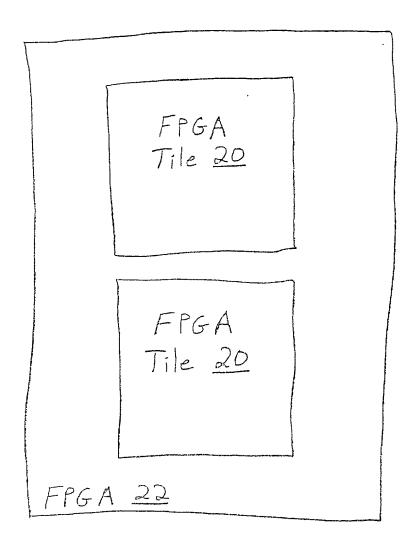


FIG. 2

Docket No.: ACT-322CIP

Page 3 of 23

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FPGA
Tile 20

FIG. 3A

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Filed: February 15, 2002

Inventors: Liu, et al. Docket No.: ACT-322CIP

Page 4 of 23

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ROM FPGA FPGA Tile 20 Tik 20 FPGA FPGA RAM Tile 20 Tik 20 FPGA 24 Other Components SOC 25

FIG. 3B

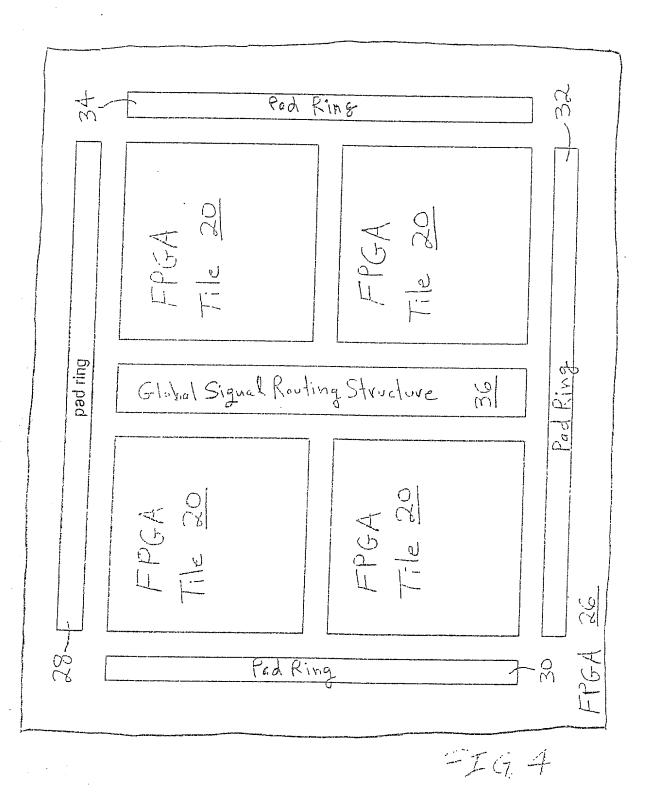
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Docket No.: ACT-322CIP

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Page 5 of 23



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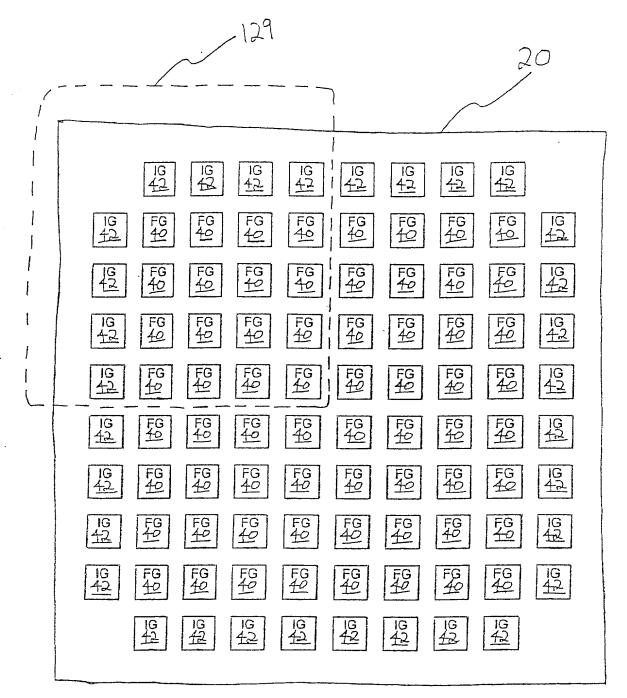
Docket No.: ACT-322CIP

Express mail: ET579963007US

Page 6 of 23

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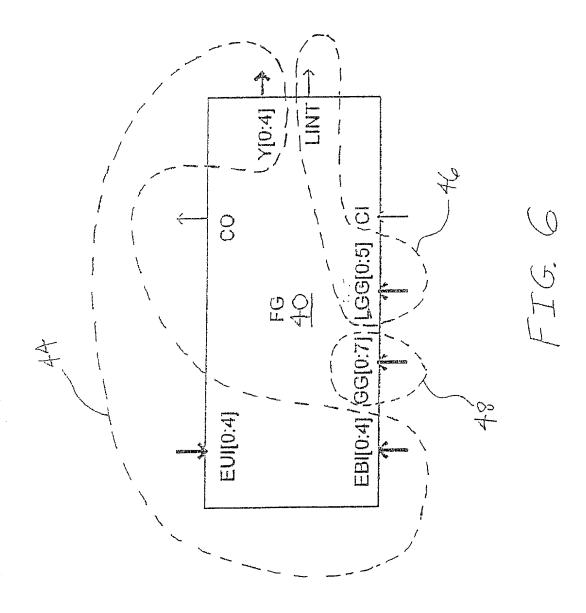
Title: FREEWAY GATE ARRAY ARCHITECTURE Filed: February 15, 2002

Inventors: Liu, et al. Docket No.: ACT-322CIP

Page 7 of 23

Express mail: ET579963007US Attorney: Michael A. Blake

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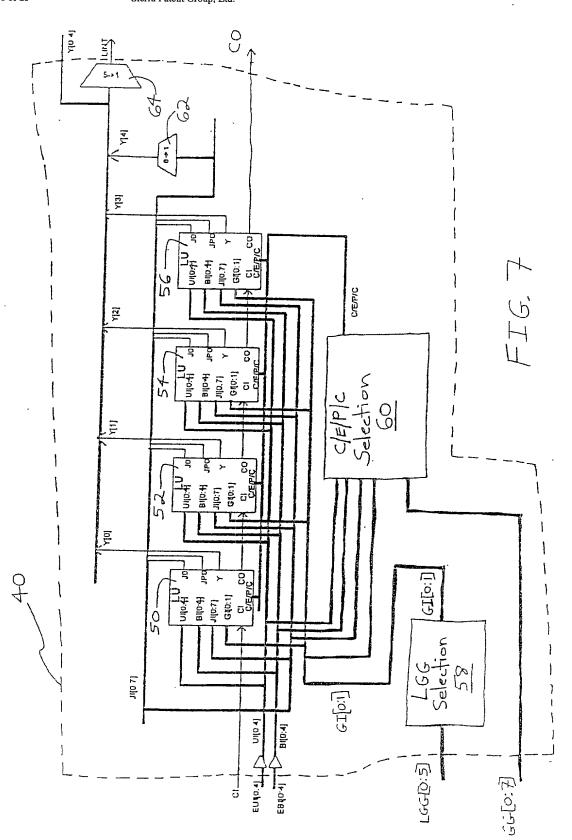


Express mail: ET579963007US Attorney: Michael A. Blake

Page 8 of 23

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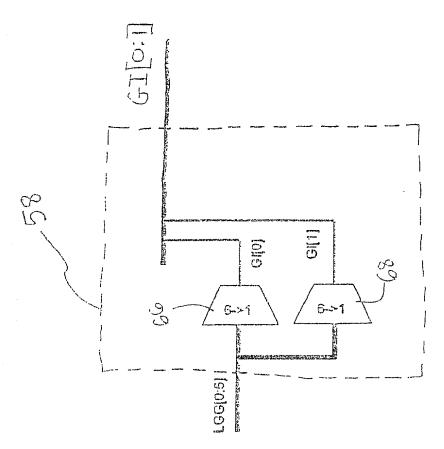
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Page 9 of 23

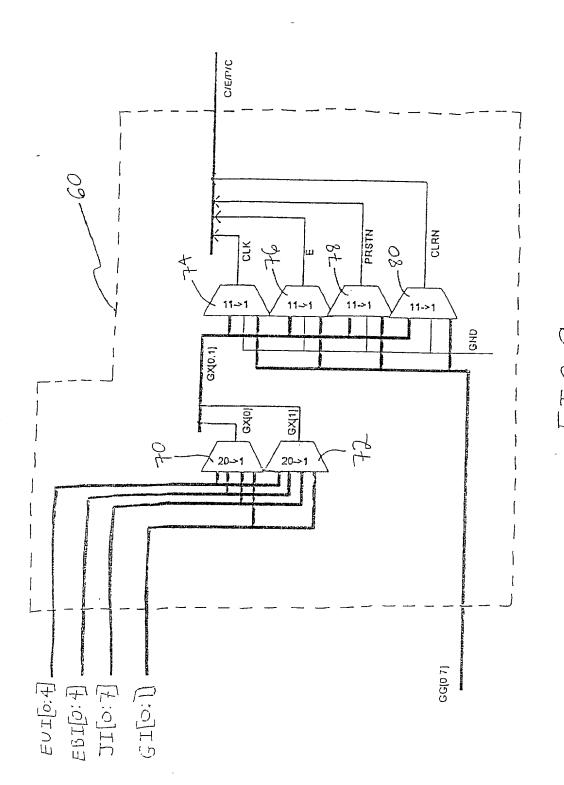
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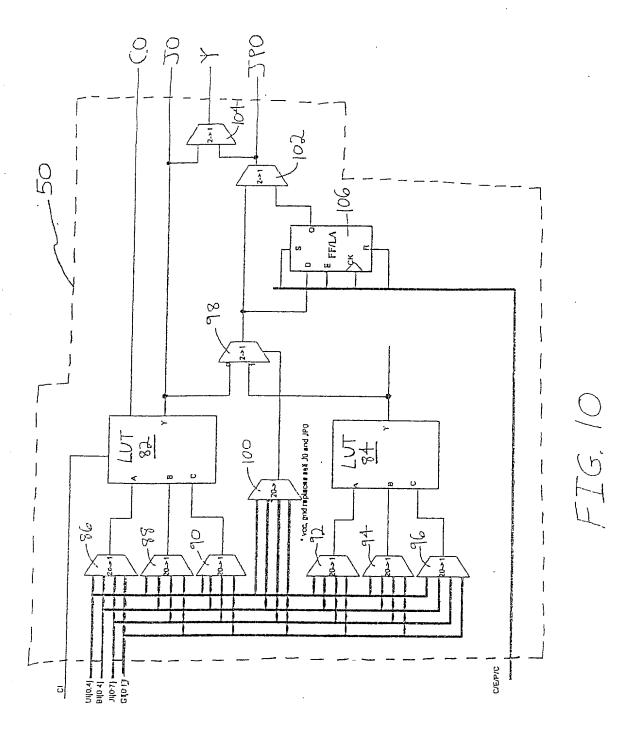
Page 10 of 23



Filed: February 15, 2002

Inventors: Liu, et al.

Docket No.: ACT-322CIP Page 11 of 23



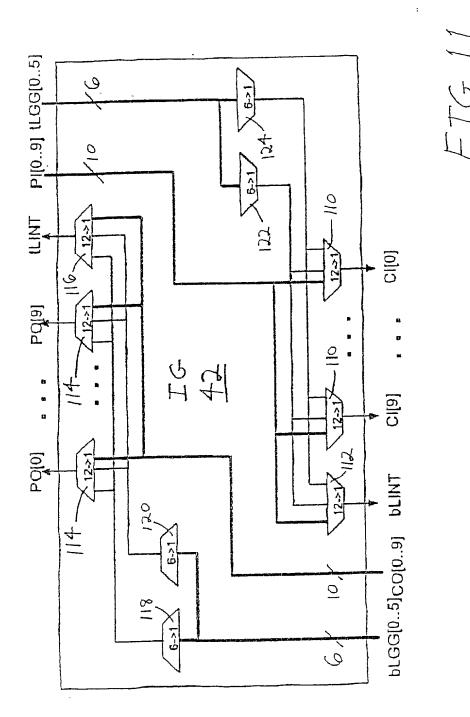
Filed: February 15, 2002

Inventors: Liu, et al. Docket No.: ACT-322CIP

Page 12 of 23

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Inventors: Liu, et al. Docket No.: ACT-322CIP

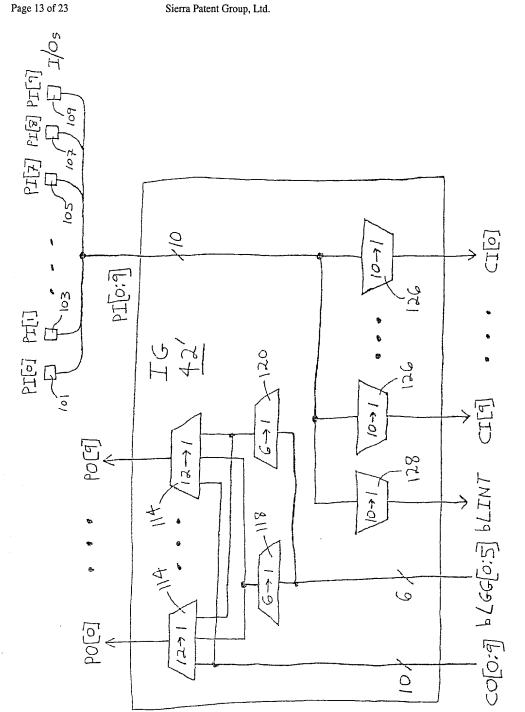


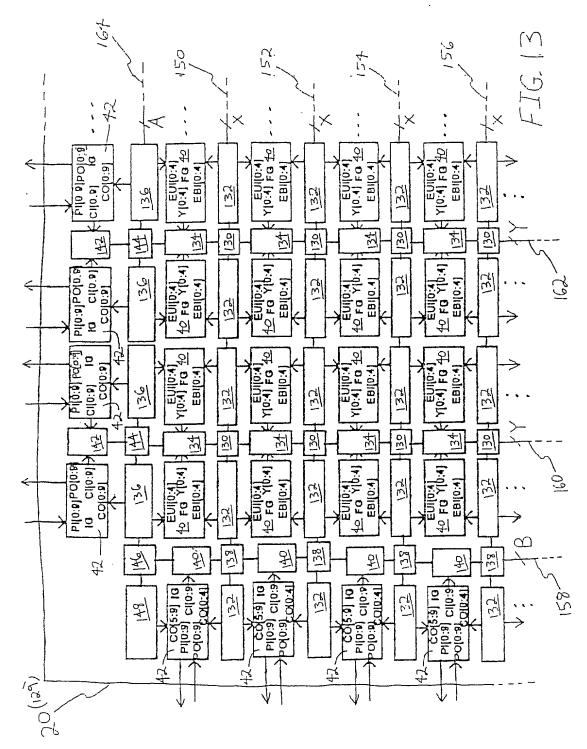
FIG. 19

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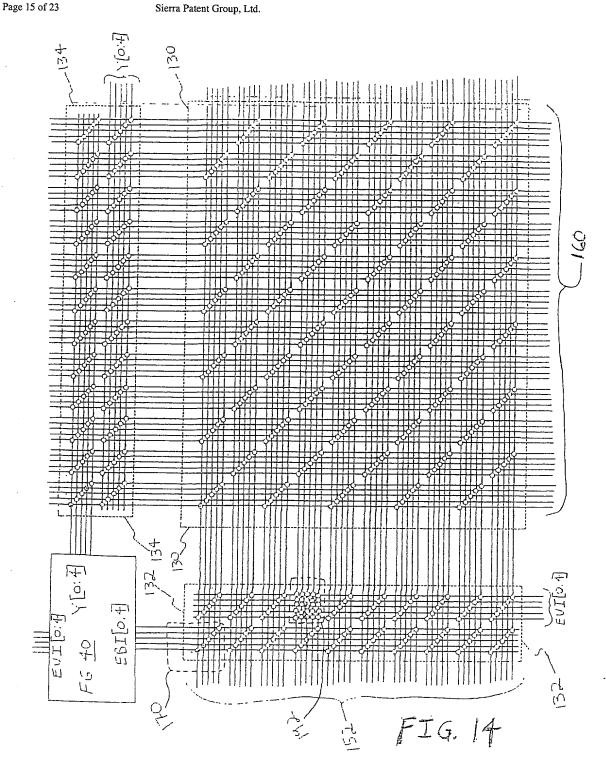
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Inventors: Liu, et al. Docket No.: ACT-322CIP

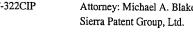


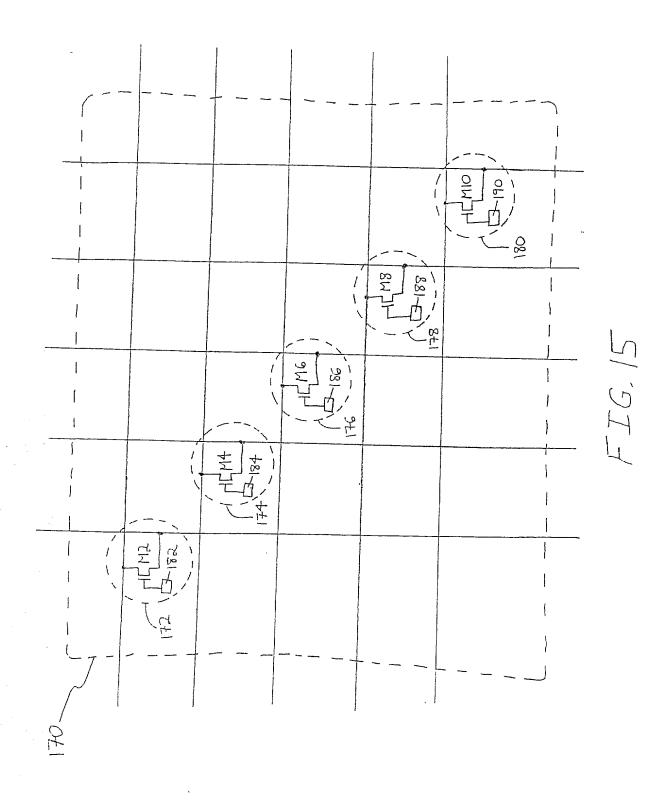
Filed: February 15, 2002

Inventors: Liu, et al.

Docket No.: ACT-322CIP Page 16 of 23

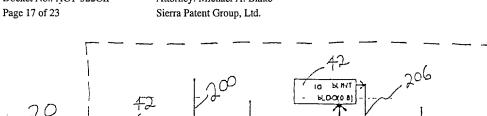
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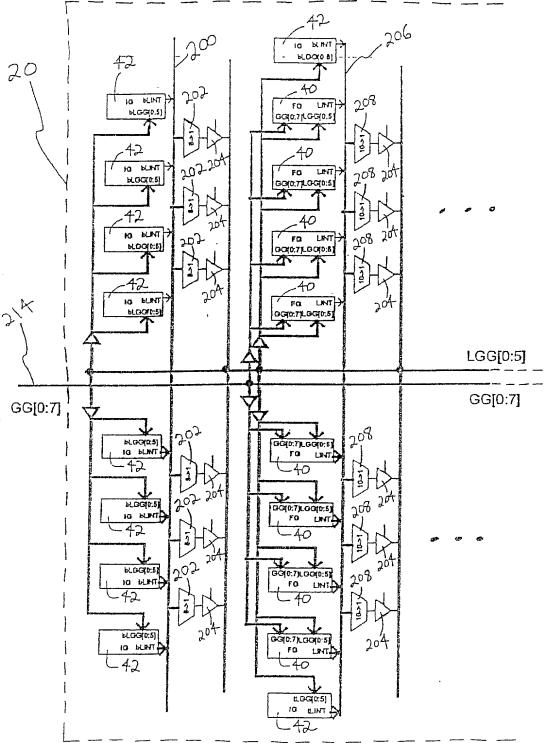


FIG. 16A

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Docket No.: ACT-322CIP

Page 18 of 23

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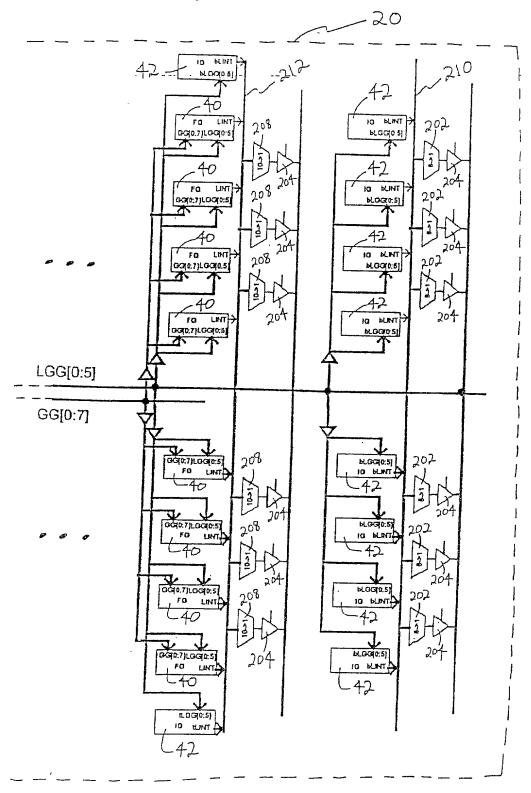
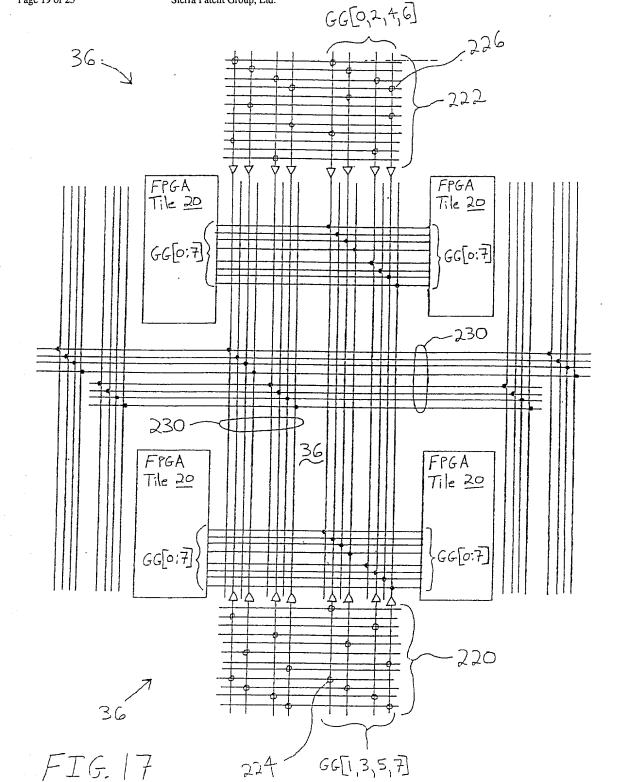


FIG. 16B

Page 19 of 23

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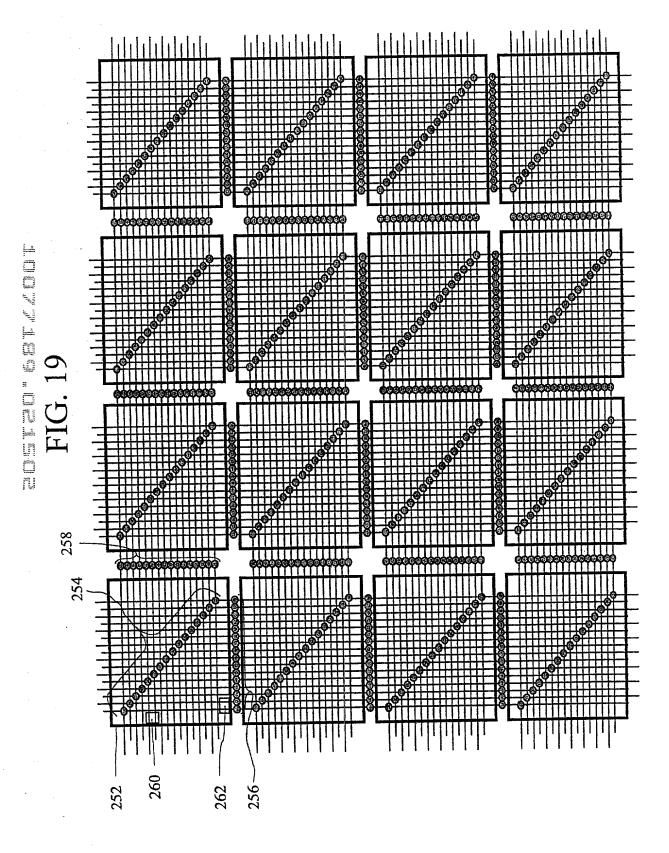


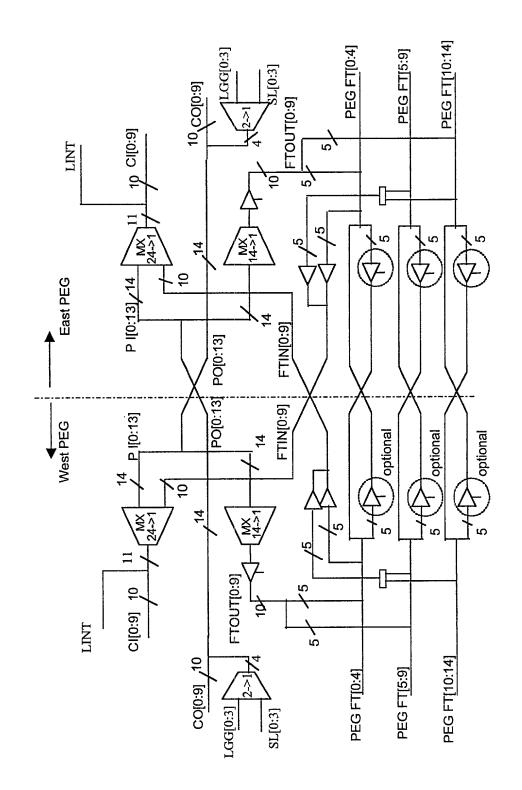
Title: FREEWAY GATE ARRAY ARCHITECTURE Filed: February 15, 2002 Inventors: Liu, et al. Express mail: ET579963007US Docket No.: ACT-322CIP Attorney: Michael A. Blake Page 20 of 23 Sierra Patent Group, Ltd. 246 Poral Poral Poral Color FFGATILE 20 #

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Docket No.: ACT-322CIP
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Page 21 of 23





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 $\mathrm{Page}\,22\,\mathrm{of}\,23$ Docket No.: ACT-322CIP Inventors: Liu, et al. Filed: February 15, 2002 Title: FREEWAY GATE ARRAY ARCHITECTURE Express mail: ET579963007US Attorney: Michael A. Blake

Page 23 of 23

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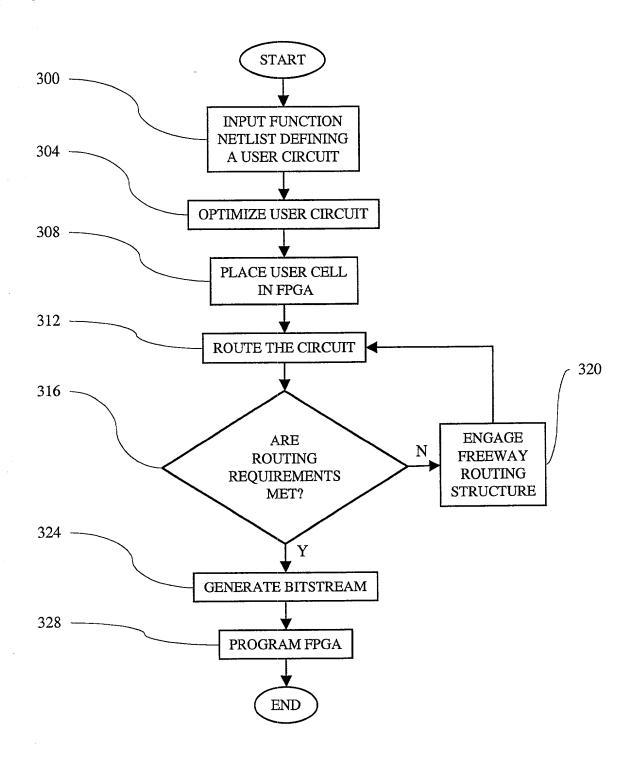


FIG. 21